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10/743,113	12/22/2003	Kyung Yun Jung	SUN-DA-114T	8491

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
3663	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,113	JUNG, KYUNG YUN	
	Examiner	Art Unit	
	JOHANNES P. MONDT	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Remarks filed 9/24/08 in response to the Office action mailed 6/25/08 form the basis for this Office action. Comments on Remarks are included below under "Response to Arguments".

Response to Arguments

2. Applicant's arguments filed 9/24/08 have been fully considered but they are not fully persuasive.

3. (a) Applicant's first argument is that by "forming a gate electrode pattern on an isolation region, there is no channel region that could be considered a lower electrode to which a first contact plug is connected". See page 2.

Examiner disagrees: isolation region 11 is only optional: see [0021]; even arguendo, only a portion of said gate electrode pattern is formed on isolation region 11, none of it directly on it, while another portion is formed directly on semiconductor substrate 10 thus forming a channel in the ON state. See Drawing 13 (a). Said channel is electrically connected to contact plug 23 through poly-plug 17. Parenthetically, examiner cannot find any reference to 13a in his rejection; presumably, applicant meant "13".

(b) Applicant's second argument is that a protective layer on the gate electrode prevents electrical contact with plug 23a.

Examiner agrees that what was advertised to be the "full text" of the computerized translation may indicate that the gate electrode is 13 and not 14 counter

to what is spelled out specifically in the Description of the Drawings, missing in said "full text" and to which reference is made. See item U on PTO-892 enclosed with this Office Action for "Description of the Drawings". Examiner regrets to have overlooked its absence in said "full text". From said "full text" the protective layer 14 is disclosed by example to be a SiN layer, which is an insulator. Depending on thickness and comprehensive coverage an electrical connection between gate (upper electrode) 13 and plug 23a exists or not. A full manual translation of Fukuzumi has been ordered from the Translator Branch at the United States Patent and Trademark Office so as to resolve the clear inconsistencies in the different parts of the translation. However, pending said manual translation the rejection over Fukuzumi is maintained and included in this action by reference, while an alternative rejection is being provided herewith based on the observation that the gate electrode as disclosed by Fukuzumi is connected to a word line, while the prior art renders obvious the routing of said word line through an overlying insulating layer. Indeed, as specifically taught by Lee et al (US 2001/0005604 A1) in art on a fuse area structure in a semiconductor device, hence analogous art, "the word line can be used as the fuse line" (see [0008] and [0047]; and see prior art Figure 1 and see Figure 8). A comparison between the actual invention by Lee et al and the alternative so suggested renders the claimed invention obvious.

The rejections provided with this Office action are based on the above considerations.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. ***Claims 1-10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloud et al (US 2002/0015322 A1) in view of Lee et al (US 2001/0005604 A1) and Noble et al (US 2002/0024083 A1).

Cloud et al teach a semiconductor device (see Abstract), comprising:

a capacitor having a bottom electrode (channel of MOSFET 210) ([0030]), a dielectric layer 213 formed on the bottom electrode, and an upper electrode (gate electrode 212 of MOSFET 210) formed on the dielectric layer, the capacitor being formed on a semiconductor substrate 211([0029]) (see Figure 2);

a first insulating layer 232 formed on the semiconductor substrate covering the capacitor;

while Cloud et al do no specifically disclose the limitation of lines 6-11 of claim 1 but instead omit details on the bitline connections altogether, it would have been obvious to include said limitation in view of Lee et al, who, in a patent application drawn

to a DRAM device (see title, abstract and "Background of the Invention") , hence art analogous to Cloud et al, teach:

a plurality of contact plugs 122, 128 formed in a plurality of via holes of the first insulating layer 120, each electrically connected to either the bottom electrode (channel of semiconductor substrate 110 (semiconductive because otherwise the gate action of 114 would not be operative in the transistor) or the upper electrode (age electrode 114), namely: electrically connected to the bottom electrode (through the source/drain regions 116 and 118) (see Figure 8; also see Figures 1 and 9-10);

a first metal wiring 124 (bitline wiring) formed on the first insulating layer 120 and connected to the bottom electrode through one of the first contact plugs (122);

a second insulating layer (either 126 or 126/136) formed on the first insulating layer.

(End of reference to teaching by Lee et al).

As shown by Lee et al, the inclusion of the limitation is nothing more than the application of standard, i.e., conventional DRAM device design employing a multi-layer metal interconnection structure (see also Figure 1 in their description of the Prior Art at the time of their filing, which also exhibits the same DRAM bitline design). The limitation is especially obvious in light of the conventional multi-layer construction of DRAM devices (see [00006]] in Lee et al) wherein examiner takes official notice that for reason of separate operating function different metal connections are separated by interlayer dielectric.

Furthermore, Cloud et al teach:

a second contact plug 230 in insulating layer 232 ([0030]) and connected to the upper electrode 212;

an anti-fuse (capacitor dielectric 222) ([0030]) [Examiner note: anti-fuse materially is nothing more than a thin dielectric layer, "anti-fuse" distinguishing only intended use] formed on the second contact plug in a second via hole, i.e., via hole in a "subsequent layer" containing capacitor 220, which would have been obviously insulating within the context of aforementioned multi-layered DRAM design; said anti-fuse or capacitor dielectric capable of providing electrical connection of a third contact plug to the second contact plug (see below for an embodiment thereof; however, it is noted that the limitation "for electrical connection to the second contact plug" constitutes only a limitation of intended use); the third contact plug here being the concave central portion of top plate 223, filling the second via hole and formed within the anti-fuse, wherein the third contact plug does not directly contact any underlying insulating layer other than said anti-fuse; and

a second metal wiring (top and side portions of top plate 213) formed on the insulating layer 232 and electrically connected to the third contact plug (through a contiguous connection) and to the anti-fuse (which it abuts and hence exerts capacitive coupling thereon).

Cloud et al do not specifically teach the limitation that the second contact plug is formed in a second insulating layer because as we have seen Cloud et al only provide an incomplete teaching of the bitline interconnect. However, following the teaching of Lee et al as referred to above, it would have been obvious to locate the capacitor well

above and separated by interlayer dielectric from the bit lines, motivation being provided by said separation of functionally independent metal parts: this is what Lee et al disclose: capacitor 130/132/134 connected to contact plug (upper portion of 128) in a second insulating layer 126 on a first insulating layer 120. The limitation would have been obvious nothing more than the application of standard, i.e., conventional DRAM device design employing a multi-layer metal interconnection structure (see also Figure 1 in their description of the Prior Art at the time of their filing, which also exhibits the same DRAM bitline design). The limitation is especially obvious in light of the conventional multi-layer construction of DRAM devices (see [00006]] in Lee et al) wherein examiner takes official notice that for reason of separate operating function different metal connections are separated by interlayer dielectric. Incorporation of the teaching by Lee et al in the semiconductor device by Cloud et al requires nothing more than combining prior art elements according to known methods to yield predictable results: the additional teaching by Lee et al only ensures placing bitline metal on a lower interlayer dielectric than the capacitor. In the invention by Cloud et al the capacitor is placed on the gate of the transistor and hence both source and drain interconnects could connect at a comparable, and lower interlayer dielectric level than the level of the capacitor, as confirmed by Noble et al (US 2002/0024083 A1) (see source line 217A and bit line 219A in vertical relation to the capacitor 220; Figure 2 and [0047]-[0049]).

On claim 2: first and second metal wiring are perpendicular to each other (word line WL and bitline BL; see Fig. 1; wordline is tied to second wiring (top plate 223) (Figure 2 and [0011]) (see also Noble et al; Figure 2 and [0047]-[0049]).

On claims 3 and 8: The device of claim 1 would necessarily have to be formed in order to function. Claim 1 fails to further limit the device of claim 1 other than simply form each of their components.

On claim 5: in the combined invention, wherein the interlayer dielectrics are taken from Lee et al, the upper surface of the third contact plug and the upper surface of the second insulating layer are at least substantially in the same horizontal plane; namely: the upper plane boundary, on the right-hand side, of 126/136 (see Figures 8-10). Applicant does not disclose the specific equality of heights, implicitly an extremely narrow range limitation, to be critical to the invention. Its incorporation in a dependent claim only is evidence to the contrary. Applicant's disclosure does not teach why the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

On claims 4 and 7: in the combined invention, the anti-fuse 222 is formed between the second contact plug 230 and the third contact plug (inner, central portion of 223) and between the second insulating layer (which, following Lee et al takes up the uppermost portion of 232) and the third contact plug (inner central portion of 223 between the vertical parts of 222).

On claims 6 and 10: the range limitation on relative width of the third contact plug to that of the second contact plug recited by claim 6 has not been disclosed as critical to applicant's invention. On the contrary, said range limitation evidently is not critical to the

invention, because claim 1 defines an acceptable invention by applicant and does not contain the limitation of said range. Applicant is reminded that Applicant's disclosure does not teach why the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al (US 6,861,686 B1) (previously so cited).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHANNES P. MONDT whose telephone number is (571)272-1919. The examiner can normally be reached on 7:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Johannes P Mondt/
Primary Examiner, Art Unit 3663